



HK32F030 Datasheet

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Preface

Purpose

This document introduces the block diagram, the memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F030 Series SOC, to help users quickly understand its features and functions.

Audience

This document is intended for:

- HK32F030 Developer
- HK32F030 Tester
- HK32F030 user

Release Notes

This document is corresponding to HK32F030 Series SOC.

Revision History

Version	Date	Description
1.0.0	2018/06/08	Initial release
1.1.0	2019/10/20	Update <i>Chapter 4 Electrical characteristics</i> .
1.2.0	2020/07/28	Update <i>Section 3.7 NVIC</i> .
1.2.1	2020/08/21	Update <i>Chapter 6 AF function and pin mapping</i> .
1.2.2	2021/06/21	Update <i>Section 2.2 Device overview</i> .
1.2.3	2021/07/30	Update <i>Section 4.2.12 ADC characteristics</i> . Added <i>Section 3.9 Reset</i> .

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1 Introduction

This document is the datasheet for HK32F030 series System-on-Chips (SOCs). HK32F030 is a family of low power microcontrollers (MCU) developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd, including:

- HK32F030x4P6
 - HK32F030F4P6
- HK32F030x6T6
 - HK32F030C6T6
 - HK32F030K6T6
- HK32F030x8T6
 - HK32F030R8T6
 - HK32F030C8T6

Please refer to HK32F030 Reference Manual for more details.

2 HK32F030 Overview

2.1 Features

- CPU core
 - ARM® Cortex®-M0 core
 - Maximum frequency: 72 MHz
 - 24-bit SysTick timer
 - Supports output the Event signal to MCU pins (to co-work with others system-on-chip CPUs)
- Operating voltage range
 - Single power supply (V_{DD}): 2.0 V to 5.5 V
- Operating temperature range: -40°C to +105°C
- Typical operating current
 - Run mode: 13.23mA/72MHz @3.3V
 - Sleep mode: 5.44mA@3.3V
 - Stop mode:
 - LDO Full-speed running: 128μA@3.3V
 - LDO low-power mode: 10μA@3.3V
 - Standby mode: 1.64μA@3.3V
- Memory
 - Up to 64 Kbytes Flash
 - When the CPU frequency is not more than 24 MHz, MCU supports zero wait state
 - Flash data security protection function (read or write protection can be set respectively)
 - Instructions and data stored in Flash can be encrypted to be protected from physical attack
 - 10-Kbyte internal SRAM (without Hardware parity function)
- Clock
 - External high-speed clock (HSE): 4 MHz to 16 MHz (typical value: 8 MHz)
 - External low-speed clock (LSE): 32.768 kHz
 - Internal high-speed clock (HSI): 8 MHz/14 MHz/56 MHz
 - Internal low-speed clock (LSI): 40 kHz
 - PLL clock
 - External clock input
- Reset
 - External pin reset
 - POR/PDR reset
 - Software reset
 - Watchdog timer reset (IWDG and WWDG)
 - Low-power mode reset
- Programmable voltage detection (PVD)
 - Adjustable 8 level thresholds of detecting voltage
 - Configurable rising/ falling edge for detecting
- GPIO

- Up to 55 GPIOs
- Each GPIO can be configured as an external interrupt input
- Provides up to 20 mA driving current
- DMA controller
 - A 5-channel DMA controller
 - Supports triggering by peripherals, such as timer, ADC, SPI, I2C, USART
- Data security
 - CRC verification hardware unit
- Data communications interfaces
 - 2 x USARTs (supports Master/Slave SPI, modem operations (CTS/RTS), ISO7816, LIN, IrDA SIR ENDEC specifications, auto-baud rate detection and wake-up features)
 - 2 x high-speed SPIs (supports a 4- to 16-bit programmable frame and the I2S protocol)
 - 2 x I2Cs (can be woken up from Stop mode, and supports Fast-mode plus (1 Mbit/s) and SMBus / PMBus.
- Timer
 - 1 x advanced PWM timers: TIM1 (total 6 PWM outputs with programmable inserted dead-times and the break function)
 - 5 x general-purpose PWM timers: TIM3/TIM14/TIM15/TIM16/TIM17
 - 1 x basic timers: TIM6
- RTC provides a clock-calendar function (MCU can be woken up from Stop/Standby mode via RTC)
- On-chip analog circuits
 - 1 x 12-bit ADC, up to 1 MSPS sampling frequency, supports automatic consecutive conversion and scan conversion (total 16 external analog input channels)
 - 1 x temperature sensor (the analog output internally connects to the ADC channel on chip)
- Fixed-point division and square root operations
 - Supports 32-bit fixed-point division, the Quotient and remainder are obtained simultaneously
 - Supports 32-bit fixed-point square root with high accuracy
- CPU trace and debug
 - SWD debug interface
- Reliability
 - Passed HBM2000V/CDM500V/MM200V/LU level test

2.2 Device overview

Table 2-1 HK32F030 series features

Features		HK32F030F4P6	HK32F030K6T6/ HK32F030C6T6	HK32F030C8T6/ HK32F030R8T6
Operating Voltage		2.0 V to 5.5 V		
Operating Temperature		-40°C to +105°C		
CPU	Core	Cortex®-M0		
	Maximum frequency	72 MHz		
Memory	Flash (Kbyte)	16	32	64
	SRAM (Kbyte)	10		

Features		HK32F030F4P6	HK32F030K6T6/ HK32F030C6T6	HK32F030C8T6/ HK32F030R8T6
DMA		5 Channels (supports ADC/SPI/I2C/USART/Timer)		
Clock	LSI	40 kHz		
	HSI	8 MHz/14 MHz/56 MHz		
	HSE	4 to 16 MHz		
	LSE	32.768 kHz		
	PLL	support		
Timer	Advanced PWM Timer	TIM1		
	General-purpose PWM timer	TIM3/TIM14/TIM15/TIM16/TIM17		
	Basic timer	TIM6		
	SysTick timer	support		
	RTC	support		
	IWDG	support		
	WWDG	support		
Peripherals	USART	1	1	2
	I2C	1	1	2
	SPI/I2S	1	1	2
	DMA	1 (5 channels)		
Analog Circuitry	ADC	1 (10 channels)	1 (10 channels)	1 (10 channels) / 1 (16 channels)
	Temperature Sensor	1		
GPIO		15	26/39	39/55
PVD		support		
DVSQ		support		
Data Security	CRC	support		
	UID	support		
Power Consumption	Run mode		13.23 mA @72MHz@3.3V	
	Sleep mode		5.44 mA@3.3V	
	Stop mode	LDO full-speed running	128 μ A@3.3V	
		LDO low-power mode	10 μ A@3.3V	
	Standby mode		1.64 μ A@3.3V	
Package		TSSOP20	LQFP32/LQFP48	LQFP48/LQFP64

3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor, which provides a MCU platform with low-cost and low-power consumption features. It delivers outstanding computational performance and an advanced system response to interrupts. With its embedded ARM Cortex-M0 core, HK32F030 family is compatible with ARM tools and software.

Take HK32F030R8T6 for example, the block diagram of HK32F030 shows as follows:

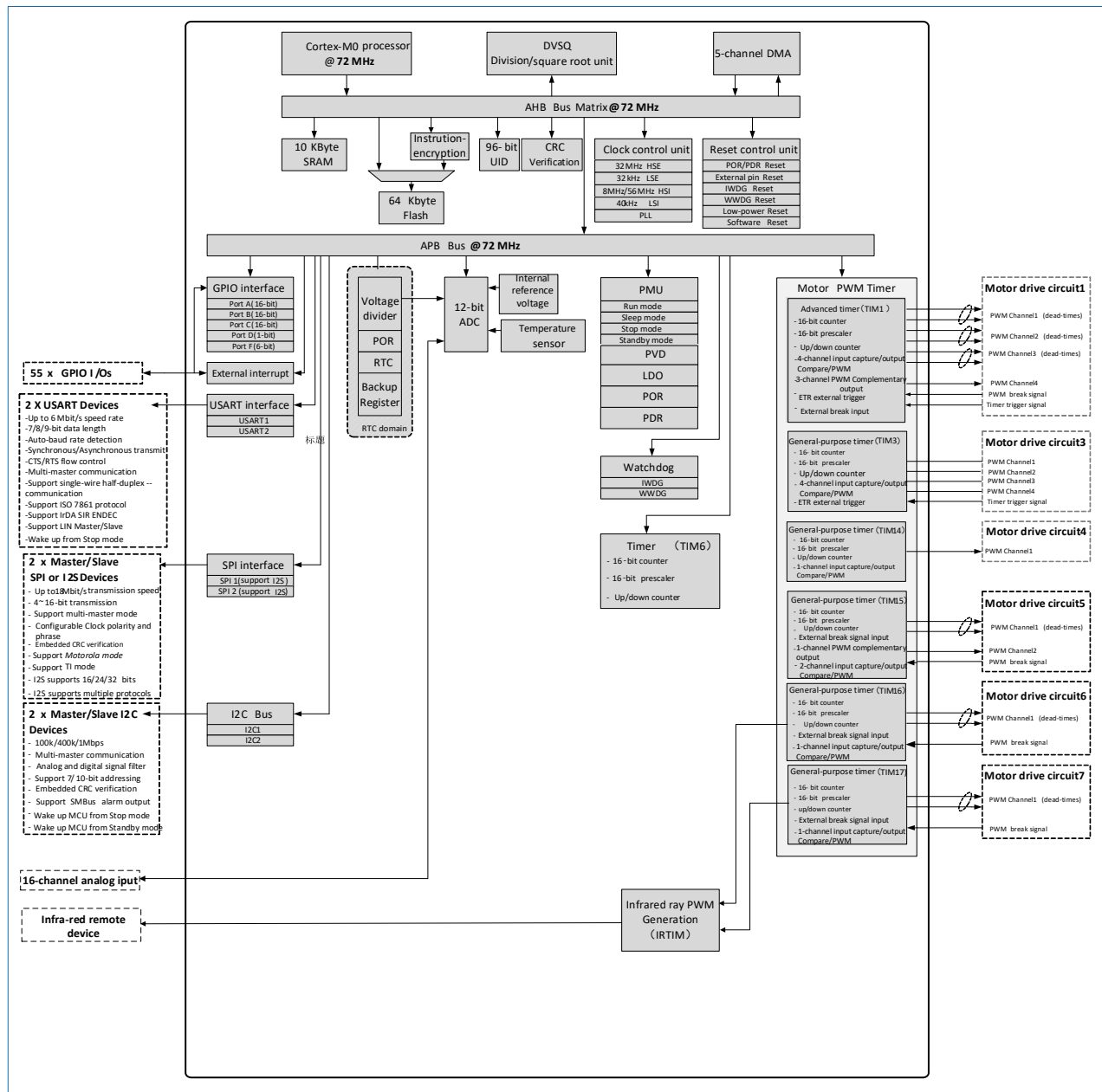


Figure 3-1 HK32F030R8T6 block diagram

3.2 Memory mapping

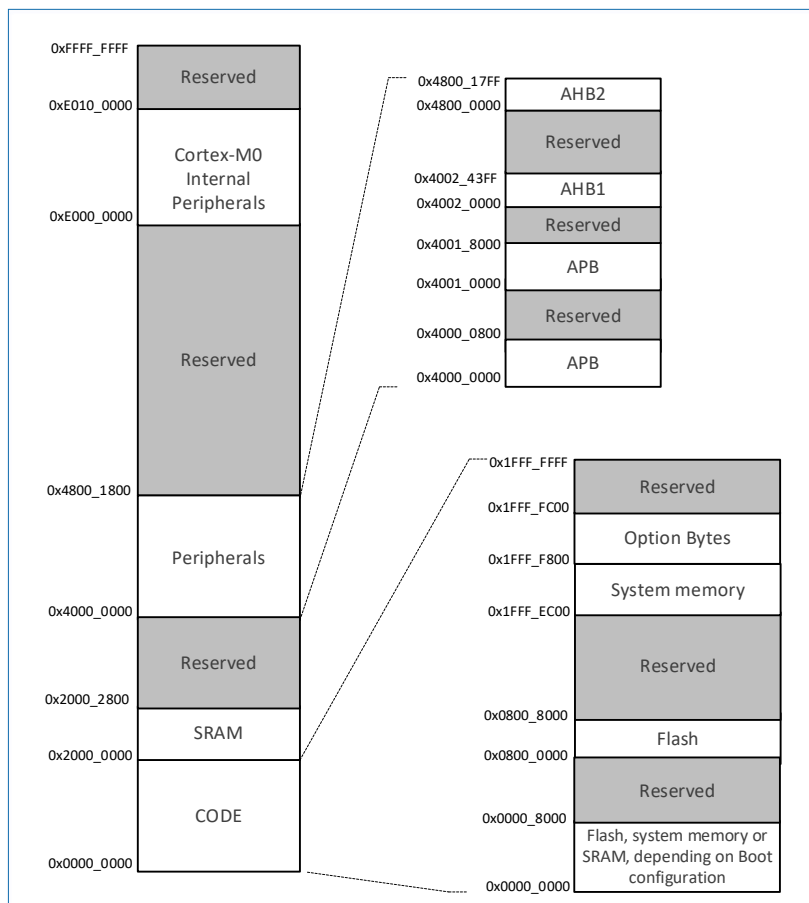


Figure 3-2 Memory mapping

3.3 Flash

HK32F030 integrates a Flash memory up to 64 Kbytes to store programs and data.

3.4 CRC calculation unit

CRC is used to verify data transmission or storage integrity. HK32F030 integrates a CRC calculation unit to reduce application processing burden and accelerate processing.

CRC calculation unit helps compute a signature of the software during runtime, and compared it with a reference signature generated at link-time and stored at a given memory location.

3.5 DVSQ unit

Division and square root calculation (DVSQ) unit features:

- Supports 32-bit signed/unsigned number division and 32-bit unsigned number square root operations
 - DVSQ unit supports only one type calculation each time, either division or square root
 - Once 32-bit signed/unsigned integer division operations complete, its quotient and the remainder are obtained simultaneously and updated in the corresponding register
 - Unsigned number square root operations can be set by software to operate with high precision
 - Division operations support MOD operating
- Pipeline design: 2-bit calculation is completed in every clock period
- Calculation time depends on data in the operation

- Supports dividing by zero interrupts and overflow interrupts

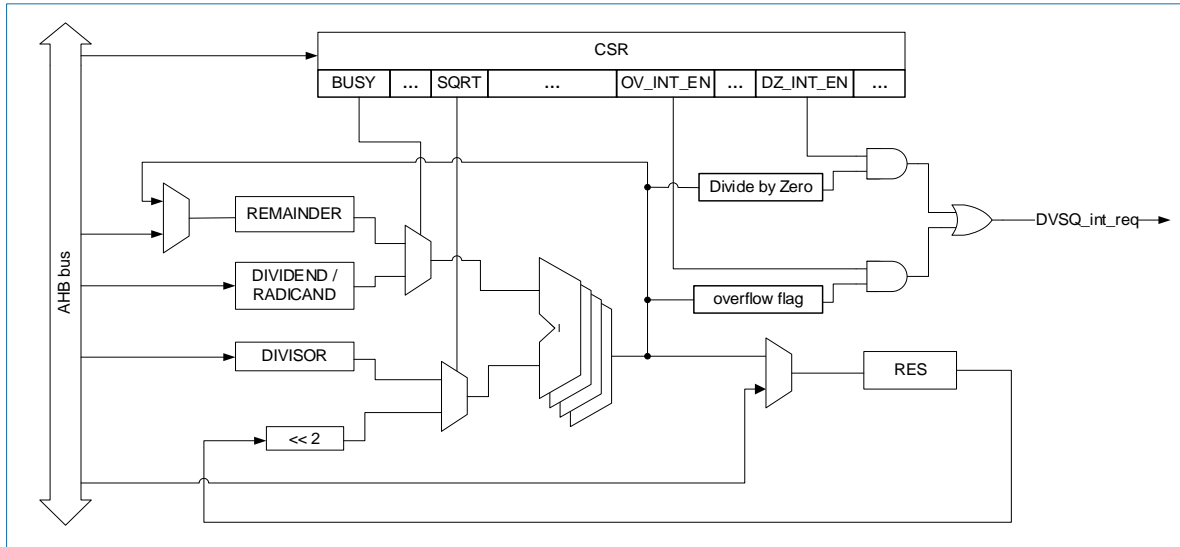


Figure 3-3 DVSQ interrupt request

3.5.1 Division operation

The value in the result register (RES) and the remainder register (REMAINDER) is always in complement form.

- For an unsigned number division operation, the value in the RES and the REMAINDER registers is positive.
- For a signed number division operation, the sign bit in the RES/the REMAINDER registers depends on the input operand.
 - If the signed bits of the divisor and dividend are different, the quotient is negative.
 - If the signed bits of the divisor and dividend are the same, the quotient is positive.

A division operation can be started through the fast or non-fast methods. The division operation flow is as follows:

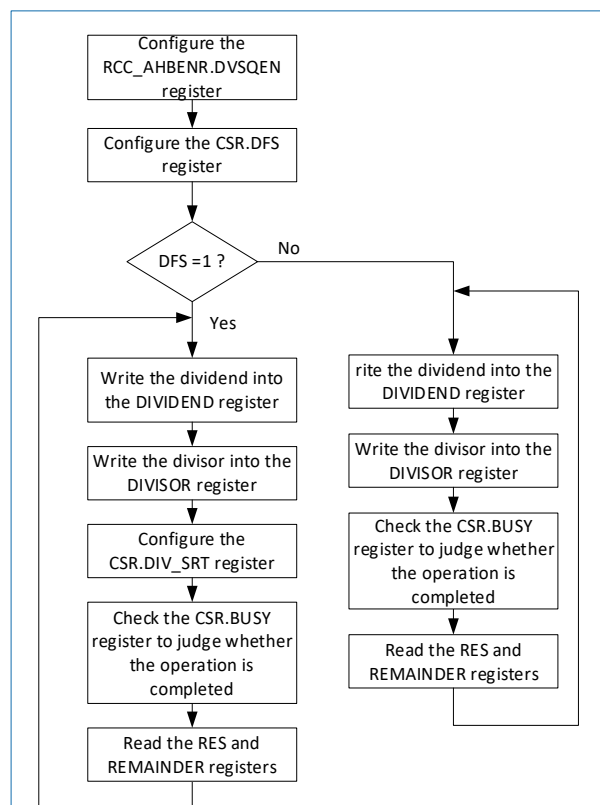


Figure 3-4 Division operation flow

Note:

- **During the division operation, the Hardware is unable to change the values in the DIVIDEND and DIVISOR registers, but software is able to. You must be careful when writing a new value into these registers. For example, when writing a value (a byte) into the DIVIDEND[7:0] field, it stores the new value. The DIVIDEND[31:8] field remains the last value of the division operation.**
- **If the division operation is set to fast-start mode, programming the DIVISOR register in a unit of byte, half-word or word starts the division operation.**

3.5.2 Square root operation

DVSQ unit supports unsigned number square root operation. The values in the RADICAND and RES registers are unsigned number. The square root operation flow is as follows:

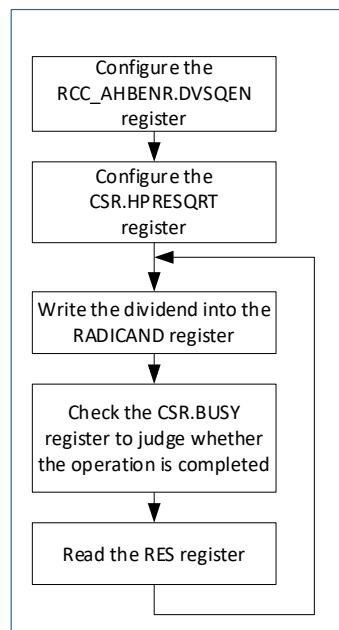


Figure 3-5 Square root operation flow

3.5.3 Interrupt

The two internal interrupt sources of the DVSQ unit share the same interrupt number. When detecting an interrupt request, the system identifies the interrupt type by reading CSR register. The interrupt types are the divided by zero interrupt or the overflow interrupt. Only one of the two interrupts occurs at a time.

- The divided by zero interrupt:
 - Enable or disable this interrupt by configuring the CSR.DZ_INT_EN bit.
 - When the divisor is 0, hardware sets the interrupt request.
 - This interrupt can be cleared through software or hardware:
 - The CSR.OV_FLAG bit is set to 0 through software.
 - Start the next division operation or square root operation.
- Signed number division overflow interrupt:
 - Enable or disable this interrupt by configuring the CSR.OV_INT_EN bit.
 - When the dividend is 0x8000_0000 and the divisor is 0xFFFF_FFFF, hardware sets the interrupt request.
 - This interrupt can be cleared through software and hardware.
 - The CSR.OV_FLAG bit is set to 0 through software.

- Start the next division operation or square root operation.

Note:

When the DVSQ unit has not completed an operation, accessing the DIVIDEND/DIVISOR/RADICAND /RES/REMAINDER registers puts the bus into the wait state. In the wait state, interrupts are disabled. Software can judge whether the RES and REMAINDER values are prepared by checking the CSR.BUSY bit.

3.6 SRAM

HK32F030 integrates a 10-Kbyte SRAM. CPU can access SRAM fast with zero wait state, which can meet the requirements of most applications.

3.7 NVIC

HK32F030 embeds a nested vectored interrupt controller (NVIC) to manage interrupt flexibly with the low interrupt latency. The NVIC can handle 32 non-maskable interrupts and 4 level priorities.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Supports for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

Table 3-1 NVIC

Position	Priority	Name	Description	Address
-	-	-	Reserved	0X0000_0000
-	-3	Fixed	Reset	0X0000_0004
-	-2	Fixed	NMI Non-maskable interrupt The RCC Clock Security System (CSS) is linked to the NMI vector.	0X0000_0008
-	-1	Fixed	HardFault All class of fault	0X0000_000C
-	3	Settable	SVCall System service call via SWI instruction	0X0000_002C
-	5	Settable	PendSV Pendable request for system service	0X0000_0038
-	6	Settable	SysTick System tick timer	0X0000_003C
0	7	Settable	WWDG Window watchdog interrupt	0X0000_0040
1	8	Settable	PVD PVD interrupt (combined EXTI lines 16)	0X0000_0044
2	9	Settable	RTC RTC global interrupt (combined EXTI lines 17, 19 and 20)	0X0000_0048
3	10	Settable	FLASH Flash global interrupt	0X0000_004C
4	11	Settable	RCC RCC global interrupt	0X0000_0050
5	12	Settable	EXTI0_1 EXTI Line[1:0] interrupts	0X0000_0054
6	13	Settable	EXTI2_3 EXTI Line[3:2] interrupts	0X0000_0058
7	14	Settable	EXTI4_15 EXTI Line[15:4] interrupt	0X0000_005C
8	15	-	- Reserved	0X0000_0060
9	16	Settable	DMA_Channel1 DMA Channel1 global interrupt	0X0000_0064

Position	Priority		Name	Description	Address
10	17	Settable	DMA_Channel2_3	DMA Channel2 and 3 global interrupts	0X0000_0068
11	18	Settable	DMA_Channel4_5	DMA Channel4 and 5 global interrupts	0X0000_006C
12	19	settable	ADC	ADC interrupts	0X0000_0070
13	20	settable	TIM1_BRK_UP_TRG_COM	TIM1 break, update, trigger and commutation interrupt	0X0000_0074
14	21	settable	TIM1_CC	TIM1 Capture Compare interrupt	0X0000_0078
15	22	-	-	Reserved	0X0000_007C
16	23	settable	TIM3	TIM3 global interrupt	0X0000_0080
17	24	settable	TIM6	TIM6 global interrupt	0X0000_0084
18	25	-	-	Reserved	0X0000_0088
19	26	settable	TIM14	TIM14 global interrupt	0X0000_008C
20	27	settable	TIM15	TIM15 global interrupt	0X0000_0090
21	28	settable	TIM16	TIM16 global interrupt	0X0000_0094
22	29	settable	TIM17	TIM17 global interrupt	0X0000_0098
23	30	settable	I2C1	I2C1 global interrupt (combined with EXTI line 23)	0X0000_009C
24	31	settable	I2C2	I2C2 global interrupt (combined with EXTI line 24)	0X0000_00A0
25	32	settable	SPI1	SPI1 global interrupt	0X0000_00A4
26	33	settable	SPI2	SPI2 global interrupt	0X0000_00A8
27	34	settable	USART1	USART1 global interrupt (combined with EXTI line 25)	0X0000_00AC
28	35	settable	USART2	USART2 global interrupt (combined with EXTI line 26)	0X0000_00B0
29	36	-	-	Reserved	0X0000_00B4
30	37	-	-	Reserved	0X0000_00B8
31	38	settable	DVSQ	DVSQ global interrupt	0X0000_00BC

3.8 EXTI

HK32F030 embeds 24 external interrupt/event controller (EXTI) lines. The trigger event of each EXTI line can be configured and masked separately. The trigger event might be a rising edge, a falling edge or both. The pending register is for maintaining states of interrupt requests. EXTI can detect a pulse, the width of which is less than the internal clock period. The external interrupt lines are up to 16.

HK32F030 embeds 24 EXTI lines. EXTI0- EXTI5 connects to IOs, the other EXTI lines can be configured to trigger the following events.

- EXTI16 connects to PVD output
- EXTI17 connects to RTC to detect an alarm event
- EXTI19 connects to RTC to detect tamper and timestamp events
- EXTI20 connects to RTC to detect a wakeup event
- EXTI23 connects to I2C1 to detect a wakeup event
- EXTI24 connects to I2C2 to detect a wakeup event
- EXTI25 connects to USART1 to detect a wake-up event
- EXTI26 connects to USART2 to detect a wake-up event

EXTI23-EXTI26 are used as internal events, without the RTSR, FTSR, SWIER and PR register. In Stop mode, EXTI23-

EXTI26 generate ERQ and IRQ signals to wake up the system by sampling the rising edge of an event.

3.9 Reset

HK32F030 supports System reset, Power reset and Backup domain reset.

3.9.1 System reset

Except for the reset flags in the RCC_CSR register and registers in the backup domains, System reset signal resets all the registers.

When any of the following events occurs, System Reset signal is generated:

- Low-level voltage on NRST pin (External Reset)
- Window watchdog counting terminates (WWDG Reset)
- Independent watchdog counting terminates (IWDG Reset)
- Software reset (SW Reset)
- Low-power consumption management reset

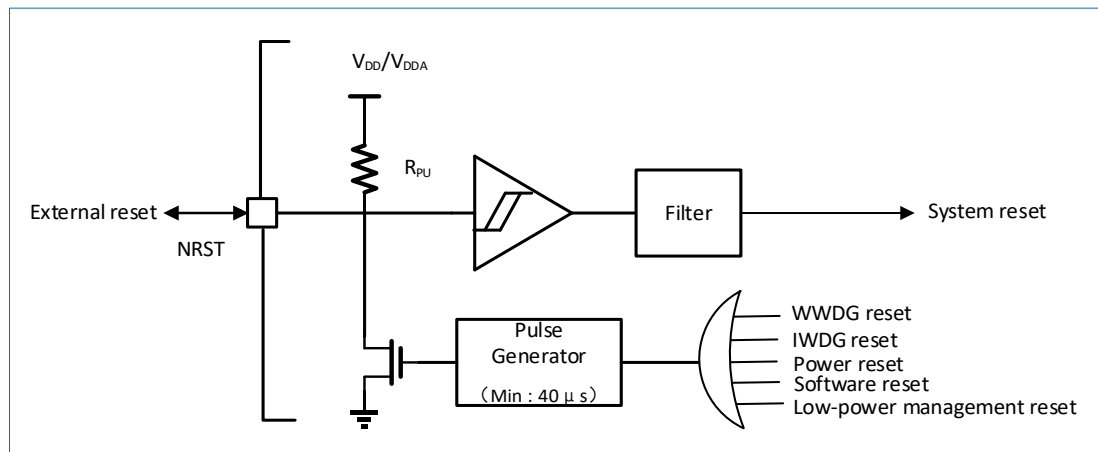


Figure 3-6 System reset

An Internal Reset signal is output via the NRST pin. A Pulse generator guarantees that each reset source produces at least 40 μs pulse latency. When NRST pin is pulled down, a reset pulse is generated for an external reset.

You can identify a reset source by checking reset state flags in the RCC_CSR register.

Table 3-2 Reset setting

Software reset	By setting the SYSRESETREQ bit to '1' or generating a Cortex-M3 interrupt to perform Software reset.
Low-power consumption management reset	To generate a low-power management reset when entering Standby/Stop mode: Set the nRST_STDBY/nRST_STOP bit in Option bytes to '1' to enable the low-power management reset function. Then, even it is in the process of entering Standby/Stop mode, the system will be reset instead of enter Standby/Stop mode.

3.9.2 Power reset

Power reset signal resets all registers except for the registers in the backup domain. The reset source acts on the reset pin, and keeps low level in the progress of reset. Reset entry vector is fixed on address 0x0000_0004.

When the following event occurs, Power reset signal is generated:

- POR/PDR reset
- Return from Standby mode

HK32F030 embeds POR/PDR circuitry. The circuitry always operates to ensure the system runs well with the power supply over than POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, MCU resets and no

external reset circuit is required.

3.9.3 Backup domain reset

Backup domain has two dedicated reset signals, which only affect the backup domain. When one following event occurs, backup domain reset signal is generated:

- Software reset: Backup domain reset signal can be generated by the BDRST bit in the RCC_BDCR register.
- When V_{DD} are not present, powering on V_{DD} resets the backup domain.

3.10 Clock

HSI and HSI14 are clocked from the same internal RC oscillator with 56MHz output frequency. Therefore, when one clock is used, you cannot shutdown the other clock to reduce the power consumption. HSI can be used as a pre-scaler input. More clock frequencies can be produced by using HSI and PLL. All on-chip clock sources (including LSI and LSE) can be selected as system clock. User can flexibly choose system clock upon the consumption and function requirement.

The following clock can be used as a CPU clock:

- 32 kHz LSE
- 40 kHz LSI
- 56 MHz HSI
- HSI
- HSI14
- 4 GPIO pins (PA0/PA4/PA13/PA14)

Note: The PCLK clock can be selected as a I2C clock source.

The clock tree is as below:

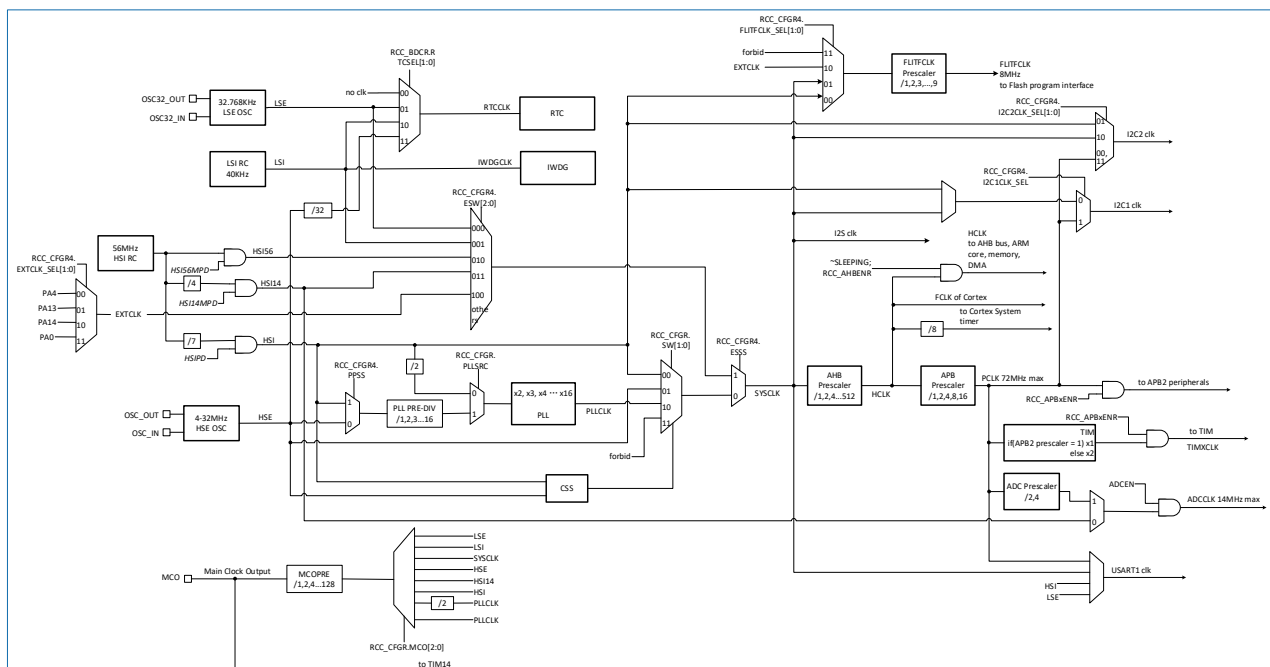


Figure 3-7 Clock tree

3.11 Boot mode

When the system starts, the Boot pin is used to select one mode from three modes:

- Boot from Flash block

- Boot from the system memory
- Boot from the internal SRAM

Boot-loader program is stored in the system memory and it can reprogram Flash via the USART1 or USART2 interfaces.

3.12 Power supply schemes

- V_{DD} : 2.0V to 5.5V

The V_{DD} pin supplies power for I/O pins and internal LDO.

- V_{DDA} : 2.0V to 5.5V

The V_{DDA} pin supplies power for ADC and temperature sensor analog circuitry.

Note:

HK32F030 does not have separate V_{BAT} pin. When the V_{DD} is present, the RTC domain works normally, and supports Standby low-power mode, illustrated as below:

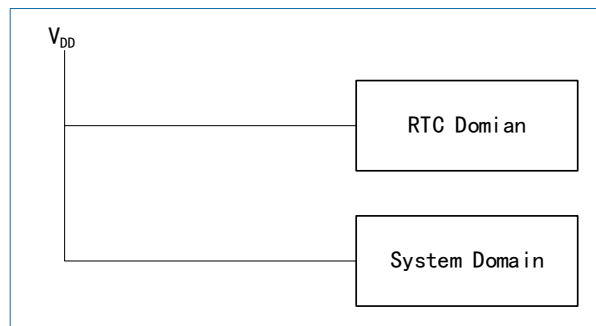


Figure 3-8 Power supply Schemes

3.13 PVD

HK32F030 integrates a programmable voltage detector (PVD). The PVD monitors V_{DD} power supply and compare it with the V_{PVD} threshold. When V_{DD} is lower or higher than the V_{PVD} threshold, an interrupt is generated. The interrupt program sends an alarm message and/or puts MCU into Safe mode. PVD is enabled by software.

3.14 Low-power modes

HK32F030 supports several low-power modes to achieve the best compromise between low power consumption, short startup time and available wake-up sources.

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

In Stop mode, MCU achieves the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all internal clocks, the PLL, the HSE/HSI oscillators are disabled. MCU can be woken up from Stop mode by any EXTI line. The EXTI line source can be any one of external I/O pins, a PVD output, a RTC alarm, a UART frame header matching event and an I2C address matching event.

- Standby mode

In Standby mode, MCU achieves the lowest power consumption. The internal LDO is off. The PLL, the HSE/HSI oscillators are disabled. In Standby mode, the content in SRAM and registers are lost except for the ones of registers in the backup domain, and Standby circuitry is still working.

MCU exits from Standby mode when an external reset (NRST), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

For more information of power consumption of different modes, please see [Table 4-6](#).

3.15 DMA

The flexible 5-channel general-purpose DMA manages transfers from memories to memories, devices to memories, and memories to devices. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Every channel has a dedicated hardware DMA request logic and can be triggered by software. Transfer sizes, source address and destination address can be set independently by software. DMA can serve for the main peripherals, such as SPI, I2C, USART, timer and ADC.

3.16 RTC

Real-time clock (RTC) contains an independent BCD timer/counter. Its features as below:

- Calendar with sub-seconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. It can synchronize the RTC with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate the quartz crystal deviation.
- Two anti-tamper detection pins with programmable filter. When a tamper event is detected, the MCU can be woken up from Stop/Standby mode.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

3.17 Independent Watchdog

Independent watchdog (IWDG) is based on a 12-bit down counter and an 8-bit pre-scaler. The IWDG is clocked from an internal independent 40 kHz RC oscillator. As it is independent from the main clock, IWDG can operate in Stop mode and Standby mode. It can be used as a watchdog to reset the system when a problem occurs, or as a free running timer for application timeout management. IWDG can be configured as a software or hardware watchdog through Option bytes. In debug mode, the counter can be frozen.

3.18 Window Watchdog

Window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the system clock and has an early warning interrupt capability. In debug mode, the counter can be frozen.

3.19 SysTick timer

SysTick timer is dedicated to the operation system as a standard down counter. It features:

- 24-bit down counter
- Auto-reload capability
- Generate a maskable interrupt when the counter reaches 0.
- Programmable clock source

3.20 Timer

HK32F030 integrates a basic timer (TIM6), 5 general-purpose timers (TIM2/TIM3/TIM4/TIM5), and an advanced timer (TIM1).

Table 3-3 Timer features

Type	Timer Name	Counter resolution	Counter type	Prescaler factor	DMA request	Break input	Capture/compare channel	Complementary output
Advanced timer	TIM1	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	Yes	4	3
General-purpose timer	TIM3	16 bits	up, down, up/down	Any integer between 1 and 65536	Yes	No	4	No
	TIM14	16 bits	up	Any integer between 1 and 65536	No	No	1	No
	TIM15	16 bits	up	Any integer between 1 and 65536	Yes	Yes	2	1
	TIM16	16 bits	up	Any integer between 1 and 65536	Yes	Yes	1	1
	TIM17	16 bits	up	Any integer between 1 and 65536	Yes	Yes	1	1
Basic timer	TIM6	16 bits	up	Any integer between 1 and 65536	Yes	No	No	No

3.20.1 Basic timer

Basic timer (TIM6) can be used as a 16-bit time base timer.

3.20.2 General-purpose timer

Every general-purpose timer can generate a PWM output and can be used as a time base.

- TIM3

TIM3 provides a 16-bit auto-reload up/down counter, a 16-bit prescaler and 4 independent channels. Every channel can be used for input capture, output compare, PWM and a single pulse output.

TIM3 can cooperate with advanced timers through Timer Linking feature for synchronization and event chaining. TIM3 supports an independent DMA request mechanism. TIM3 is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14 and TIM15

TIM14 and TIM15 provide a 16-bit auto-reload up counter, a 16-bit pre-scaler. TIM14 has a channel for input capture, output compare, PWM and a single pulse output. In debug mode, the counter can be frozen. TIM14 cannot generate a DMA request, but TIM15 can.

- TIM16 and TIM17

Both TIM16 and TIM17 provide a 16-bit auto-reload up counter, a 16-bit pre-scaler. Each of them has a channel for input capture, output compare, PWM and a single pulse output. TIM16 and TIM17 have complementary PWM outputs with programmable inserted dead-times and can generate DMA requests. In debug mode, the counter can be frozen.

3.20.3 Advanced timer

The advanced timers (TIM1) can be seen as a three-phase PWM generator multiplexed on 6 channels, and used

as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If configured as a standard 16-bit timer, an advanced timer has the same functions as the general-purpose timer. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Because most of its internal structure is the same as that of a general-purpose timer, the advanced timer can work together with general-purpose timers via Timer Link feature for synchronization or event chaining. In debug mode, the counter can be frozen.

3.21 I2C bus

Two I2C bus interfaces can work as a master or as a slave and support standard, fast mode and fast mode plus (up to 1Mbit/s).

The I2C interface supports 7-bit or 10-bit addressing mode. It supports double-slave address addressing in 7-bit slave mode.

The I2C interfaces embed a CRC generator/checker hardware.

The I2C interfaces have address resolution protocol (ARP) capability and support host notification protocol, packet error checking (PEC) generation/verification, timeout verification and ALERT protocol management. They can be served by DMA and they support SMBus V2.0/PMBus 1.1.

I2C has a clock which is independent from the CPU clock domain, thus the I2C is able to wake up MCU from Stop mode when the addresses match.

Table 3-4 Programmable analog and digital noise filter

	Analog filter	Digital filter
Suppressing pulse width	≥ 50 ns	1 -15 programmable I2C peripheral clocks
Advantage	operate in Stop mode	1. Additional filtering capability and standard request 2. Stable length
Disadvantage	Vary with temperature, voltage and technology	-

3.22 USART

HK32F030 embeds 2 universal synchronous/asynchronous receiver and transmitter (USART1/USART2), with maximum communication frequency up to 6Mbit/s. These interfaces provide asynchronous communications, IrDA SIR ENDEC support, multi-processor communications, single-wire half-duplex communications and have LIN Master/Slave capability.

All the USART interfaces provide hardware management of the CTS, RTS and RS485 DE signals, Smart Card mode (ISO 7816 compliant).

USART can be served by DMA.

Table 3-5 USART1 features

features	USART1/USART2
Hardware flow control	Yes
DMA continuous transmission	Yes
Multi-processor communications	Yes

features	USART1/USART2
Synchronous mode	Yes
Smart Card mode	Yes
Single-wire half-duplex communications	Yes
IrDA SIR ENDEC	Yes
LIN Master/Slave mode	Yes
Dual clock domain and wake up from Stop mode	Yes
Receiver timeout interrupt	Yes
ModBus communications	Yes
Auto-baudrate detection	Yes
Driver enable	Yes

3.23 SPI

HK32F030 has 2 SPI interfaces. In master or slave mode, full-duplex and half-duplex communicate speed is up to 18 Mbit/s. The 3-bit pre-scaler gives 8 master mode frequencies. Each frame can be configured to 4 or 16 bits.

The 2 SPI interfaces can operate in I2S mode. The standard I2S interfaces (duplex with SPI) support 4 different audio standards, can run in master or slave half-duplex modes. The interfaces can be configured to 16, 24, or 32 bits transmission. The interfaces support 16-bit or 32-bit digital resolution, which is synchronized by dedicated signal. They support audio sampling from 8 kHz to 192 kHz through an 8-bit programmable Linear pre-scaler. When it is configured as a master, its main clock can output 256 times sampling frequency to an external audio component.

Table 3-6 SPI features

Features	SPI1/SPI2
Hardware CRC computation	Yes
RX/TX FIFO	Yes
NSS pules mode	Yes
I2S mode	Yes
TI mode	Yes

3.24 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate functional interface. Most of GPIO pins are shared with digital or analog peripherals. All GPIOs are high current capable. The I/Os alternate function configuration can be locked in order to avoid spurious writing to the I/O registers.

3.25 ADC

HK32F030 embeds a 12-bit ADC. The ADC has up to 16 external channels, performing conversions in single-shot or scan mode. In scan mode, the conversion on the selected group of analog input executes automatically.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be served by DMA. The analog watchdog feature allows to monitor the converted voltage of one channel, multiple channels, and selected channels. When the monitored voltage is lower or higher than the

preset threshold, an interrupt is generated. The events generated by general-purpose timers and advanced timers can connect to the ADC start trigger and injection trigger respectively, to allow the application to synchronize A/D conversion and timers.

ADC can sample the 1/2 on the V_{DD} pin.

3.26 Temperature sensor

Temperature sensor generates a voltage that varies linearly to temperature. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into digital value.

3.27 Internal reference voltage

Internal reference voltage (V_{REFINT}) provides a stable voltage for ADC and comparator. V_{REFINT} pin is connected to the ADC_IN17 input channel. Access mode supports read only.

3.28 Debug interface

Build-in ARM SWJ-DP interface, which combined with a single wire debug interface, to realize the connection between serial single wire debug interfaces (SWDIO and SWCLK).

4 Electrical characteristics

4.1 Absolute maximum values

Note :

- Stresses above the absolute maximum rating listed in [Table 4-1](#) and [Table 4-17](#) may cause permanent damage to the device.
- Exposure to maximum permitted conditions for extended periods may affect device reliability.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})	-0.5	6.0	V
V_{IN}	Input voltage on pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
$ \Delta V_{DDx} $	Variation between different V_{DD} Power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variation between different V_{DD} ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$I_{INJ(PIN)}^{(2)}$	Injected current on pins ⁽³⁾	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) ⁽⁴⁾	±25	

- All main power (V_{DD} , V_{DDA}) and Ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
- Negative injected current disturbs the analog performance of the device.
- When $V_{IN} > V_{DD}$, a positive injected current is induced. When $V_{IN} < V_{SS}$, a negative injected current is induced, and the injected current must be limited to the permitted range.
- When several I/Os are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.1.3 Thermal characteristics

Table 4-3 Thermal characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-45 to +150	°C
T_J	Maximum junction temperature	+125	

4.2 Operation conditions

4.2.1 General operation conditions

Table 4-4 General operation conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	72	
f_{PCLK2}	Internal APB2 clock frequency	0	72	
V_{DD}	Standard operating voltage	2	5.5	V
V_{DDA}	Analog operating voltage ⁽¹⁾	2	5.5	V
T	Operating temperature	-40	+105	°C

(1). V_{DDA} can be lower than V_{DD} , for example, $V_{DD}=5V$, $V_{DDA}=3.3V$; $V_{DD}=3.3V$, $V_{DDA}=2.5V$, ADC works normally.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0]=000	2.183	2.188	2.196	V
		PLS[2:0]=001	2.286	2.289	2.298	
		PLS[2:0]=010	2.393	2.399	2.407	
		PLS[2:0]=011	2.502	2.508	2.518	
		PLS[2:0]=100	2.621	2.629	2.639	
		PLS[2:0]=101	2.726	2.733	2.745	
		PLS[2:0]=110	2.839	2.846	2.855	
		PLS[2:0]=111	2.958	2.969	2.979	
	Programmable voltage detector level selection (falling edge)	PLS[2:0]=000	2.116	2.119	2.125	
		PLS[2:0]=001	2.208	2.211	2.220	
		PLS[2:0]=010	2.305	2.310	2.320	
		PLS[2:0]=011	2.399	2.406	2.416	
		PLS[2:0]=100	2.506	2.512	2.521	
		PLS[2:0]=101	2.596	2.602	2.613	
		PLS[2:0]=110	2.693	2.701	2.710	
		PLS[2:0]=111	2.798	2.805	2.817	

4.2.3 Operating current

Table 4-6 Operating current characteristics

Mode	Conditions	VDD@25° C			Unit
		2.0V	3.3V	5.0V	
Run Mode	HCLK=72MHz, 3 wait periods for Flash read operation, APB clock is enabled (cache enable)	21.505	22.63	22.85	mA
	HCLK=72MHz, 3 wait periods for Flash read operation, APB clock is disabled (cache enable)	12.908	13.232	13.301	mA
	HCLK = HSE (8MHz), 0 wait period for Flash read operation, APB clock is enabled (cache enable).	3.151	3.418	3.533	mA

Mode	Conditions	VDD@25° C			Unit
		2.0V	3.3V	5.0V	
	HCLK = HSE (8MHz), 0 wait period for Flash read operation, APB clock is disabled (cache enable).	2.316	2.559	2.653	mA
	HCLK = LSI (40 kHz)	196	208	212	μA
	HCLK =LSE (32.768 kHz)	190	205	215	μA
Sleep Mode	HCLK = 72 MHz, APB clock is disable	5.199	5.441	5.483	mA
	HCLK = HSI (8 MHz), APB clock is disable	0.778	0.845	0.937	mA
Stop Mode	LDO operates at full speed, HSE/HSI/LSE is disabled.	126	128	130	μA
	LDO low-power state, HSE/HSI/LSE is disabled.	9.22	10.26	12.47	μA
Standby Mode	LSI and LSE are off.	1.13	1.64	3.17	μA
	RTC with LSI and IWDG on	-	2.7	-	μA
	RTC with LSE (32.768 kHz)	-	2.6	-	μA

4.2.4 HSE clock characteristics

Table 4-7 HSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f _{HSE_ext}	External clock source frequency	-	1	8	25	MHz
V _{HSEH}	OSN_IN input pin high level voltage	-	0.7V _{DD}	-	V _{DD}	V
V _{HSEL}	OSN_IN input pin low level voltage		V _{SS}	-	0.3V _{DD}	
T _{w(HSE)}	OSN_IN high or low time		5	-	-	ns
T _{r(HSE)} / T _{f(HSE)}	OSN_IN rise or fall time		-	-	20	
C _{in(HSE)}	OSN_IN input capacitance	-	-	5	-	pF
DuCy _(HSE)	Duty cycle	-	45	-	55	%

4.2.5 LSE clock characteristics

Table 4-8 LSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
F _{LSE_ext}	External clock source frequency	-	-	32.768	1000	kHz
V _{LSEH}	OSN32_IN input pin high level voltage	-	0.7V _{DD}	-	V _{DD}	V
V _{LSEL}	OSN32_IN input pin low level voltage		V _{SS}	-	0.3V _{DD}	
T _{w(LSE)}	OSN32_IN high or low time		450	-	-	ns
T _{r(LSE)} / T _{f(LSE)}	OSN32_IN rise or fall time		-	-	50	
C _{in(LSE)}	OSN32_IN input capacitance	-	-	5	-	pF
DuCy _(LSE)	Duty cycle	-	30	-	70	%

4.2.6 High-speed internal (HSI) RC oscillator

Table 4-9 HSI RC oscillator characteristics

Symbol	Description	Conditions		Min	Typ	Max	Unit	
f _{HSI}	Frequency	-		-	8	-	MHz	
DuCy _(HSI)	Duty cycle	-		45	-	55	%	
ACC _(HSI)	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-1	-	1		
		Factory calibrated	T _A =-40 to +105°C	-2	-	2.5		%
			T _A =-40 to +85°C	-1.5	-	2.2		%
			T _A =0 to +70°C	-1.3	-	2		%
			T _A =25°C	-1.1	-	1.8		%
Tsu _(HSI)	HSI oscillator startup time	V _{SS} ≤ V _{IN} ≤ V _{DD}		1	-	2	μs	
IDD _(HSI)	HSI oscillator power consumption	-		-	80	100	μA	

4.2.7 Low-speed internal (LSI) RC oscillator

Table 4-10 LSI RC oscillator characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
f_{LSI}	Frequency	30	40	60	kHz
$T_{\text{su}(\text{LSI})}$	LSI oscillator startup time	-	-	85	μs
$\text{IDD}_{(\text{LSI})}$	LSI oscillator power consumption	-	0.65	1.2	μA

4.2.8 PLL characteristics

Table 4-11 PLL characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
$f_{\text{PLL_IN}}$	PLL Input clock	1	8.0	25	MHz
	PLL input clock duty	40	-	60	%
$f_{\text{PLL_OUT}}$	PLL multiplier output clock	16	-	72	MHz
t_{LOCK}	PLL Lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.9 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Description	Value			Unit
		Min	Typ	Max	
T_{PROG}	Half-word programming time	-	25	-	μs
	A word programming time	-	33	-	μs
T_{ERASE}	Half-page erase time	-	9.2	-	ms
	Page erase time	-	4.6	-	ms

Symbol	Description	Value			Unit
		Min	Typ	Max	
	Mass erase time		38	-	ms
IDD _{PROG}	Half-byte programming current	-	-	5	mA
IDD _{ERASE}	Page/mass erase time	-	-	2	mA
IDD _{READ}	Supply current@24MHz (read mode)	-	2	3	mA
	Supply current@1MHz (read mode)	-	0.25	0.4	mA
V _{IL}	Input low level voltage	-	-	0.1V _{DD}	V
V _{IH}	Input high level voltage	0.9V _{DD}	-	-	V
V _{OL}	Output low level voltage	-	-	0.1V _{DD}	V
V _{OH}	Output high level voltage	0.9V _{DD}	-	-	V
N _{END}	Endurance	1	-	-	kcycles
t _{RET}	Data retention	20	-	-	year

4.2.10 I/O port characteristics

Table 4-13 I/O static characteristics

Symbol	Description	Conditions	Value			Unit
			Min	Typ	Max	
V _{IH}	Input high level voltage	V _{DD} > 2V	0.42*(V _{DD} -2V)+1V	-	5.5	V
		V _{DD} ≤ 2V			5.2	
V _{IL}	Input low level voltage	-	-0.3	-	0.32*(V _{DD} -2V) + 0.75V	V
V _{hys}	Schmitt trigger voltage hysteresis	-	5%V _{DD}	-	-	mV
I _{Ikg}	Input leakage current	V _{IN} = 5V	-	-	3	μA
R _{PU}	Weak pull-up equivalent resistor	V _{IN} = V _{SS}	30	40	50	KΩ
R _{PD}	Weak pull-down equivalent resistor	V _{IN} = V _{DD}	30	40	50	KΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

Table 4-14 Output voltage AC characteristics

Mode	Symbol	Description	Conditions	Min	Max	Unit
10	f _{max(I/O)out}	Max frequency	C _L = 50 pF, V _{DD} = 2.0 V to 5.5V	-	2	MHz
	t _{f(I/O)out}	Output high to low level fall time		-	125	ns
	t _{r(I/O)out}	Output low to high level rise time		-	125	
01	f _{max(I/O)out}	Max frequency	C _L = 50 pF, V _{DD} = 2 V to 5.5 V	-	10	MHz
	t _{f(I/O)out}	Output high to low level fall time		-	25	ns
	t _{r(I/O)out}	Output low to high level rise time		-	25	
11	f _{max(I/O)out}	Max frequency	C _L =30pF, V _{DD} =2.7V to 5.5V	-	50	MHz
			C _L =50pF, V _{DD} =2.7V to 5.5V	-	30	
			C _L =50pF, V _{DD} =2V to 2.7V	-	20	
	t _{f(I/O)out}	Output high to low level fall time	C _L =30pF, V _{DD} =2.7V to 5.5V	-	5	ns
			C _L =50pF, V _{DD} =2.7V to 5.5V	-	8	
			C _L =50pF, V _{DD} =2V to 2.7V	-	12	
	t _{r(I/O)out}	Output low to high level rise time	C _L =30pF, V _{DD} =2.7V to 5.5V	-	5	ns

Mode	Symbol	Description	Conditions	Min	Max	Unit
			$C_L = 50\text{pF}$, $V_{DD} = 2.7\text{V to } 5.5\text{V}$	-	8	
			$C_L = 50\text{pF}$, $V_{DD} = 2\text{V to } 2.7\text{V}$	-	12	

4.2.11 TIM timer characteristics

Table 4-15 TIM pin input characteristics

Symbol	Description	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIM} \times CLK$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIM \times CLK}/2^{(1)}$	MHz
Res_{TIM}	Timer resolution	-	16	bit
$T_{counter}$	16-bit counter clock period when selecting an internal clock	1	65536	$T_{TIM} \times CLK$
T_{MAX_COUNT}	Maximum possible count	-	65536x65536	$T_{TIM} \times CLK$

(1). $f_{TIM \times CLK} = 72\text{ MHz}$

4.2.12 ADC characteristics

Table 4-16 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC analog power supply	-	2.0	3.3	5.5	V
INL	Integral nonlinearity (The max result of the actual conversion point subtracting the actual conversion line)	$f_{ADC} = 14\text{ MHz}$, $R_{AIN} < 10\text{ k}\Omega$, Test after calibration: $V_{DDA} = 2.4 \sim 3.6\text{V}$	-1.5	-	+1.5	LSB
DNL	Differential nonlinearity (Max conversion error)	$f_{ADC} = 14\text{ MHz}$, $R_{AIN} < 10\text{ k}\Omega$, Test after calibration: $V_{DDA} = 2.4 \sim 3.6\text{V}$	-1	-	+1	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_s^{(2)}$	Sampling rate	-	0.05	-	1	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 14\text{ MHz}$	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
$R_{AIN}^{(2)}$	External input impedance	-	-	-	50	k Ω
$R_{ADC}^{(2)}$	Sampling switch resistance	-	-	-	1	k Ω
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	-	5	pF
$t_{CAL}^{(2)}$	ADC calibration time	$f_{ADC} = 14\text{ MHz}$	5.9			μs
		-	8.3			$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14\text{ MHz}$	0.196			μs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12\text{ MHz}$	0.219			μs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14} = 14\text{ MHz}$	0.188	-	0.259	μs
$Jitter_{ADC}$	ADC trigger conversion jitter	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
$t_s^{(1)}$	Sampling time	$f_{ADC} = 14\text{ MHz}$	0.107		17.1	μs

Symbol	Description	Conditions	Min	Typ	Max	Unit
			1.5		239.5	1/f _{ADC}
t _{STAB} ⁽¹⁾	Stabilization time	-	14			μs
t _{CONV} ⁽¹⁾	Total conversion time (including sampling time)	f _{ADC} = 14 MHz, 12-bit resolution	1	-	18	μs
		12-bit resolution	14 to 252 (t _{CONV} =sampling time t _s + successive approximation time 12.5)			1/f _{ADC}

4.2.13 Temperature sensor characteristics

Table 4-17 Temperature sensor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Sensor gain	-	-	3.92	-	mV/°C

5 Pinout and pin description

HK32F030 is offered in four packages: LQFP64/LQFP48/LQFP32/TSSOP20.

5.1 LQFP64

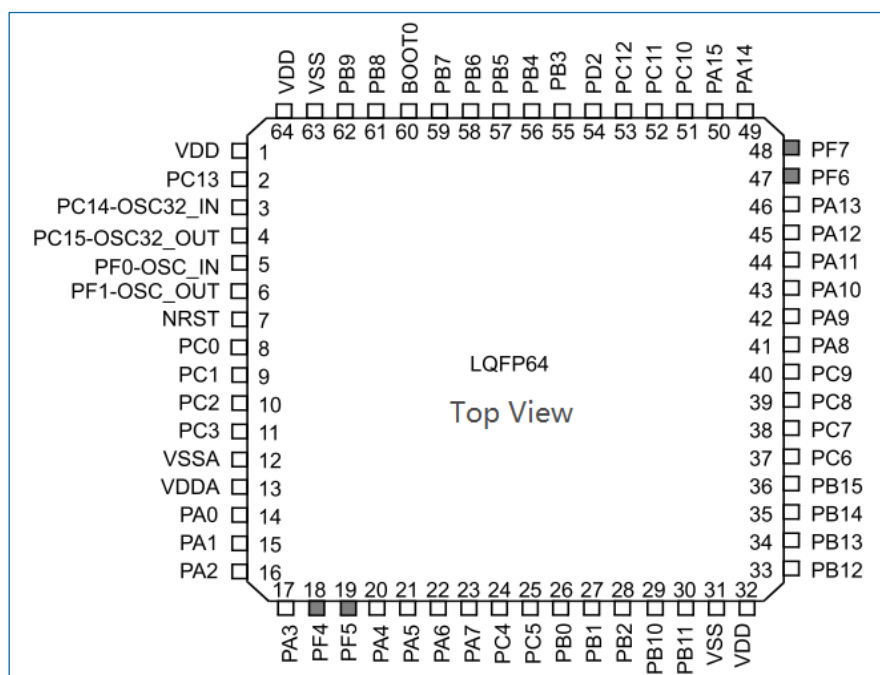


Figure 5-1 LQFP64 package pinout

5.2 LQFP48

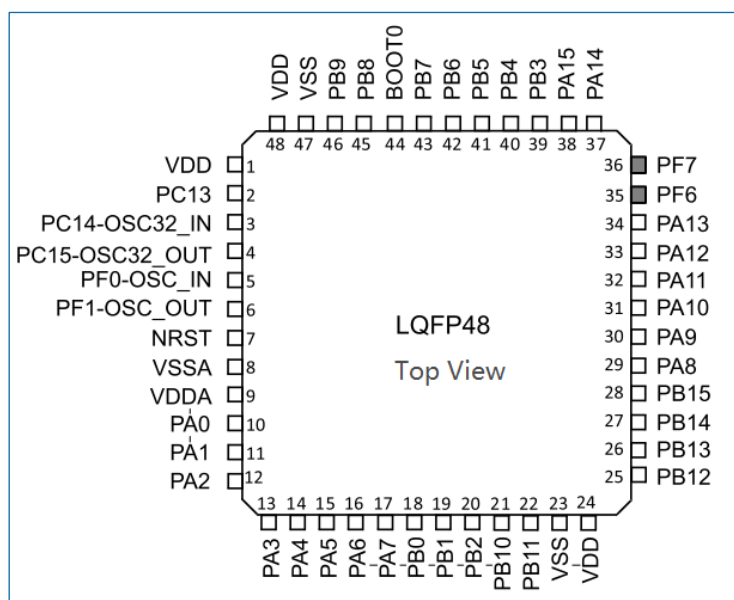


Figure 5-2 LQFP48 package pinout

5.3 LQFP32

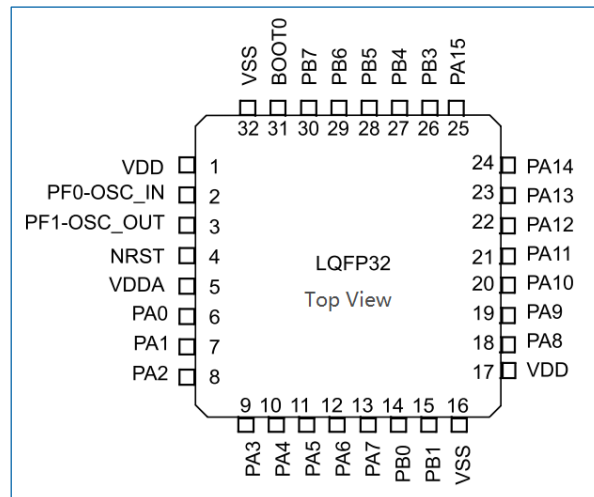


Figure 5-3 LQFP32 package pinout

5.4 TSSOP20

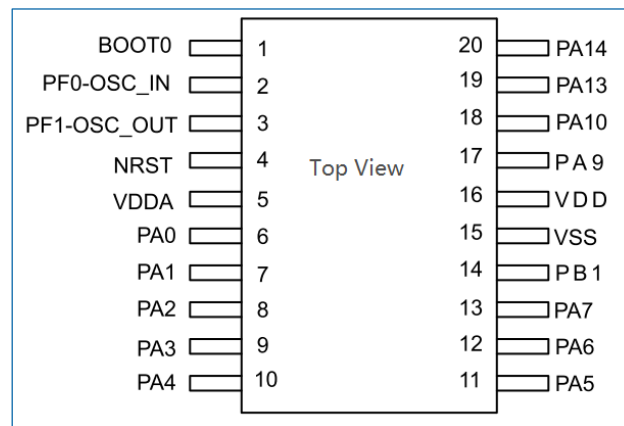


Figure 5-4 TSSOP20 package pinout

5.5 Pin description

Table 5-1 shows pin description of the four packages.

Table 5-1 HK32F030 pin descriptions

Pin number				Pin Name (Function after reset)	Pin type	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20			Default functions	Alternate functions
1	1	-	-	VDD	S ⁽³⁾	Power Supply	
2	2	-	-	PC13	I/O	-	RTC_TAMP1 RTC_TS RTC_OUT WKUP2
3	3	-	-	PC14	I/O	-	OSC32_IN
4	4	-	-	PC15	I/O	-	OSC32_OUT
5	5	2	2	PF0	I/O	I2C1_SDA	OSC_IN
6	6	3	3	PF1	I/O	I2C1_SCL	OSC_OUT

Pin number				Pin Name (Function after reset)	Pin type	Pin functions	
LQFP64	LQFP48	LQFP32	TSOP20			Default functions	Alternate functions
7	7	4	4	NRST	I/O	Device reset input / internal reset output (active low)	
8	-	-	-	PC0	I/O	EVENTOUT	ADC_IN10
9	-	-	-	PC1	I/O	EVENTOUT	ADC_IN11
10	-	-	-	PC2	I/O	EVENTOUT SPI2_MISO	ADC_IN12
11	-	-	-	PC3	I/O	EVENTOUT SPI2_MOSI	ADC_IN13
12	8	-	-	VSSA	S	Analogy ground	
13	9	5	5	VDDA	S	Analogy Power Supply	
14	10	6	6	PA0	I/O	USART1_CTS ⁽¹⁾ USART2_CTS ⁽²⁾	ADC_IN0 RTC_TAMP2 WKUP1 CKI_4
15	11	7	7	PA1	I/O	USART1_RTS ⁽¹⁾ USART2_RTS ⁽²⁾ EVENTOUT TIM15_CH1N	ADC_IN1
16	12	8	8	PA2	I/O	USART1_TX ⁽¹⁾ USART2_TX ⁽²⁾ USART1_RX ⁽¹⁾ USART2_RX ⁽²⁾ TIM15_CH1	ADC_IN2
17	13	9	9	PA3	I/O	USART1_TX ⁽¹⁾ USART2_TX ⁽²⁾ USART1_RX ⁽¹⁾ USART2_RX ⁽²⁾ TIM15_CH2	ADC_IN3
18	-	-	-	PF4	I/O	EVENTOUT	-
19	-	-	-	PF5	I/O	EVENTOUT	-
20	14	10	10	PA4	I/O	SPI1_NSS USART1_CK ⁽¹⁾ USART2_CK ⁽²⁾ TIM14_CH1	ADC_IN4 CKI_1
21	15	11	11	PA5	I/O	SPI1_SCK	ADC_IN5
22	16	12	12	PA6	I/O	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 EVENTOUT	ADC_IN6
23	17	13	13	PA7	I/O	SPI1_MOSI TIM3_CH2 TIM14_CH1 TIM1_CH1N TIM17_CH1	ADC_IN7

Pin number				Pin Name (Function after reset)	Pin type	Pin functions	
LQFP64	LQFP48	LQFP32	TSOP20			Default functions	Alternate functions
						EVENTOUT MCO	
24	-	-	-	PC4	I/O	EVENTOUT	ADC_IN14
25	-	-	-	PC5	I/O	-	ADC_IN15
26	18	14	-	PB0	I/O	TIM3_CH3 TIM1_CH2N EVENTOUT	ADC_IN8
27	19	15	14	PB1	I/O	TIM3_CH4 TIM14_CH1 TIM1_CH3N	ADC_IN9
28	20	-	-	PB2	I/O	I2C1_SMBA ⁽¹⁾ I2C2_SMBA ⁽²⁾	-
29	21	-	-	PB10	I/O	I2C1_SCL ⁽¹⁾ I2C2_SCL ⁽²⁾ SPI2_SCK	-
30	22	-	-	PB11	I/O	I2C1_SDA ⁽¹⁾ I2C2_SDA ⁽²⁾ EVENTOUT	-
31	23	16	-	VSS	I/O	Ground	
32	24	17	16	VDD	I/O	Digital power supply	
33	25	-	-	PB12	I/O	SPI1_NSS ⁽¹⁾ SPI2_NSS ⁽²⁾ TIM1_BKIN EVENTOUT I2C2_SMBA	-
34	26	-	-	PB13	I/O	SPI1_SCK ⁽¹⁾ SPI2_SCK ⁽²⁾ TIM1_CH1N I2C2_SCL	-
35	27	-	-	PB14	I/O	SPI1_MISO ⁽¹⁾ SPI2_MISO ⁽²⁾ TIM1_CH2N TIM15_CH1 I2C2_SDA	-
36	28	-	-	PB15	I/O	SPI1_MOSI ⁽¹⁾ SPI2_MOSI ⁽²⁾ TIM1_CH3N TIM15_CH1N TIM15_CH2	RTC_REFIN
37	-	-	-	PC6	I/O	TIM3_CH1	-
38	-	-	-	PC7	I/O	TIM3_CH2	-
39	-	-	-	PC8	I/O	TIM3_CH3	-
40	-	-	-	PC9	I/O	TIM3_CH4	-
41	29	18	-	PA8	I/O	USART1_CK	-

Pin number				Pin Name (Function after reset)	Pin type	Pin functions	
LQFP64	LQFP48	LQFP32	TSOP20			Default functions	Alternate functions
						TIM1_CH1 EVENTOUT MCO	
42	30	19	17	PA9	I/O	USART1_TX ⁽¹⁾ USART1_RX ⁽¹⁾ TIM1_CH2 TIM15_BKIN I2C1_SCL MCO	-
43	31	20	18	PA10	I/O	USART1_TX ⁽¹⁾ USART1_RX ⁽¹⁾ TIM1_CH3 TIM17_BKIN I2C1_SDA	-
44	32	21	-	PA11	I/O	USART1_CTS TIM1_CH4 EVENTOUT I2C2_SCL	-
45	33	22	-	PA12	I/O	USART1_RTS TIM1_ETR EVENTOUT I2C2_SDA	-
46	34	23	19	PA13	I/O	IR_OUT SWDIO	CKI_2
47	35	-	-	PF6	I/O	I2C1_SCL ⁽¹⁾ I2C2_SCL ⁽²⁾	-
48	36	-	-	PF7	I/O	I2C1_SDA ⁽¹⁾ I2C2_SDA ⁽²⁾	-
49	37	24	20	PA14	I/O	USART1_TX ⁽¹⁾ USART1_RX ⁽¹⁾ USART2_TX ⁽²⁾ USART2_RX ⁽²⁾ SWCLK	CKI_3
50	38	25	-	PA15	I/O	SPI1_NSS USART1_RX ⁽¹⁾ USART1_TX ⁽¹⁾ USART2_RX ⁽²⁾ USART2_TX ⁽²⁾ EVENTOUT	-
51	-	-	-	PC10	I/O	-	-
52	-	-	-	PC11	I/O	-	-
53	-	-	-	PC12	I/O	-	-
54	-	-	-	PD2	I/O	TIM3_ETR	-
55	39	26	-	PB3	I/O	SPI1_SCK EVENTOUT	-

Pin number				Pin Name (Function after reset)	Pin type	Pin functions	
LQFP64	LQFP48	LQFP32	TSOP20			Default functions	Alternate functions
56	40	27	-	PB4	I/O	SPI1_MISO TIM3_CH1 EVENTOUT TIM17_BKIN	-
57	41	28	-	PB5	I/O	SPI1_MOSI I2C1_SMBA TIM16_BKIN TIM3_CH2	-
58	42	29	-	PB6	I/O	I2C1_SCL USART1_TX USART1_RX TIM16_CH1N	-
59	43	30	-	PB7	I/O	I2C1_SDA USART1_TX USART1_RX TIM17_CH1N	-
60	44	31	1	Boot0	I	Boot memory selection	
61	45	-	-	PB8	I/O	I2C1_SCL TIM16_CH1	-
62	46	-	-	PB9	I/O	I2C1_SDA IR_OUT TIM17_CH1 EVENTOUT SPI2_NSS	-
63	47	32	15	VSS	S	Ground	
64	48	1	16	VDD	S	Digital power supply	

(1). Only HK32F030x4 and HK32F030x6 support the default function(s).

(2). Only HK32F030x8 supports the default function(s).

(3). I=input, O=output, I/O= input/output, S=supply.

Note: Unless otherwise specified, all I/Os are set to float input in the process of reset or after reset.

6 Function description

6.1 AF function and pin mapping

Table 6-1 GPIOA Port Alternate Function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
PA0	-	USART1_CTS ⁽¹⁾ / USART2_CTS ⁽²⁾	-	-	-	-	-	-
PA1	EVENTOUT	USART1_RTS ⁽¹⁾ / USART2_RTS ⁽²⁾	-	-	-	TIM15_CH1N	-	-
PA2	TIM15_CH1	USART1_TX ⁽¹⁾ / USART1_RX ⁽¹⁾⁽³⁾	-	-	-	-	-	-
		USART2_TX ⁽²⁾ / USART2_RX ⁽²⁾⁽³⁾						
PA3	TIM15_CH2	USART1_RX ⁽¹⁾ / USART1_TX ⁽¹⁾⁽³⁾	-	-	-	-	-	-
		USART2_RX ⁽²⁾ / USART2_TX ⁽²⁾⁽³⁾						
PA4	SPI1_NSS I2S1_WS	-	-	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK I2S1_CK	-	-	-	-	-	-	-
PA6	SPI1_MISO I2S1_MCK	TIM3_CH1	TIM1_BKIN_N	-	-	TIM16_CH1	EVENTOUT	HIS_TRIM_DONE
PA7	SPI1_MOSI I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	MCO
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	TIM15_BKIN_N	USART1_TX/ USART1_RX ⁽³⁾	TIM1_CH2	-	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN_N	USART1_RX/ USART1_TX ⁽³⁾	TIM1_CH3	-	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	I2C2_SCL	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETRIN	-	-	I2C2_SDA	-	-
PA13	SWDIO	IRTIM_IROUT	-	-	-	-	-	-
PA14	SWCLK	USART1_TX ⁽¹⁾ / USART1_RX ⁽¹⁾⁽³⁾	-	-	-	-	-	-
		USART2_TX ⁽²⁾ / USART2_RX ⁽²⁾⁽³⁾						
PA15	SPI1_NSS I2S1_WS	USART1_RX ⁽¹⁾ / USART1_TX ⁽¹⁾⁽³⁾	-	EVENTOUT	-	-	-	-
		USART2_RX ⁽²⁾ / USART2_TX ⁽²⁾⁽³⁾						

(1). Only HK32F030x4 and HK32F030x6 support the alternate function(s).

(2). Only HK32F030x8 supports the alternate function(s).

- (3). When USART_CTRL2.SWAP==1, the USART TX and USART RX of same group can be exchanged, for example the USART1_TX and USART1_RX can be exchanged.

Table 6-2 GPIOB Port Alternate Function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF15
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	-
PB2	-	-	-	-	-	-	-	I2C1_SMBA (1)/ I2C2_SMBA (x8)
PB3	SPI1_SCK I2S1_CK	EVENTOUT	-	-	-	-	-	-
PB4	SPI1_MISO I2S1_MCK	TIM3_CH1	EVENTOUT	-	-	TIM17_BKIN	-	-
PB5	SPI1_MOSI I2S1_SD	TIM3_CH2	TIM16_BKIN_N	I2C1_SMB A	-	-	-	-
PB6	USART1_TX/ USART1_RX ⁽¹⁾	I2C1_SCL	TIM16_CH1 N	-	-	-	-	-
PB7	USART1_RX/ USART1_TX ⁽¹⁾	I2C1_SDA	TIM17_CH1 N	-	-	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	-	-	-	-	-
PB9	IRTIM_IROUT	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS I2S2_WS	-	-
PB10	-	I2C1_SCL(1)/ I2C2_SCL(x8)	-	-	-	SPI2_SCK I2S2_CK	-	-
PB11	EVENTOUT	I2C1_SDA(1)/ I2C2_SDA(x8)	-	-	-	-	-	-
PB12	SPI1_NSS/I2S1_WS (1) SPI2_NSS/I2S2_WS (x8)	EVENTOUT	TIM1_BKIN_N	-	-	TIM15_BKIN	-	I2C2_SMBA
PB13	SPI1_SCK/I2S1_CK (1) SPI2_SCK/I2S2_CK (x8)	-	TIM1_CH1N	-	-	I2C2_SCL	-	-
PB14	SPI1_MISO/I2S1_MCK (1) SPI2_MISO/I2S2_MCK (x8)	TIM15_CH1	TIM1_CH2N	-	-	I2C2_SDA	-	-
PB15	SPI1_MOSI/I2S1_SD(1) SPI2_MOSI/I2S2_SD (x8)	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	-

- (1). When USART_CTRL2.SWAP==1, the USART TX and USART RX of same group can be exchanged, for example the USART1_TX

and USART1_RX can be exchanged.

Table 6-3 GPIOC Port Alternate Function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	EVENTOUT	-	-	-	-	-	-	-
PC1	EVENTOUT	-	-	-	-	-	-	-
PC2	EVENTOUT	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-
PC3	EVENTOUT	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-
PC4	EVENTOUT	-	-	-	-	-	-	-
PC5	-	-	-	-	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-
PC10	-	-	-	-	-	-	-	-
PC11	-	-	-	-	-	-	-	-
PC12	-	-	-	-	-	-	-	-
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 6-4 GPIOD Port Alternate Function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD2	TIM3_ETRIN	-	-	-	-	-	-	-

Table 6-5 GPIOF Port Alternate Function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	I2C1_SDA	-	-	-	-	-	-
PF1	-	I2C1_SCL	-	-	-	-	-	-
PF4	EVENTOUT	-	-	-	-	-	-	-
PF5	EVENTOUT	-	-	-	-	-	-	-
PF6	-	I2C1_SCL ⁽¹⁾ I2C2_SCL ⁽²⁾	-	-	-	-	-	-
PF7	-	I2C1_SDA ⁽¹⁾ I2C2_SDA ⁽²⁾	-	-	-	-	-	-

(1). Only HK32F030x4 and HK32F030x6 support the alternate function(s).

(2). Only HK32F030x8 supports the alternate function(s).

6.2 USART pin mapping

Table 6-6USART pin mapping

Pin Name	Mapping function	HK32F030F4P6	HK32F030C6T6 HK32F030K6T6	HK32F030R8T6 HK32F030C8T6
PA2/PA3	USART1	● ⁽¹⁾	●	- ⁽²⁾
PA9/PA10		●	●	●

Pin Name	Mapping function	HK32F030F4P6	HK32F030C6T6 HK32F030K6T6	HK32F030R8T6 HK32F030C8T6
PA14/PA15	USART2	●	●	-
PB6/PB7		●	●	●
PA2/PA3		-	-	●
PA9/PA10		-	-	-
PA14/PA15		-	-	●
PB6/PB7		-	-	-

The symbol “●” means the pin alternate functions are supported in the MCU(s).

The symbol “-” means the pin alternate functions are not supported in the MCU(s).

6.3 I2C pin mapping

Table 6-7 I2C pin mapping

Pin Name	Mapping function	HK32F030F4P6	HK32F030C6T6 HK32F030K6T6	HK32F030R8T6 HK32F030C8T6
PF0/PF1	I2C1	●	●	●
PB10/PB11		●	●	-
PB13/PB14		-	-	-
PA9/PA10		●	●	●
PA11/PA12		-	-	-
PF6/PF7		●	●	-
PB6/PB7		●	●	●
PB8/PB9		●	●	●
PF0/PF1	I2C2	-	-	-
PB10/PB11		-	-	●
PB13/PB14		●	●	●
PA9/PA10		-	-	-
PA11/PA12		●	●	●
PF6/PF7		-	-	●
PB6/PB7		-	-	-
PB8/PB9		-	-	-

The symbol “●” means the pin alternate functions are supported in the MCU(s).

The symbol “-” means the pin alternate functions are not supported in the MCU(s).

6.4 SPI pin mapping

Table 6-8 SPI pin mapping

Pin Name	Mapping function	HK32F030F4P6	HK32F030C6T6 HK32F030K6T6	HK32F030R8T6 HK32F030C8T6
PC2/PC3/PB10/PB9	SPI1/I2S1	-	-	-
PA4/PA5/PA6/PA7		●	●	●
PB12/PB13/PB14/PB15		●	●	-
PA15/PB3/PB4/PB5		●	●	●

Pin Name	Mapping function	HK32F030F4P6	HK32F030C6T6 HK32F030K6T6	HK32F030R8T6 HK32F030C8T6
PC2/PC3/PB10/PB9	SPI2/I2S2	●	●	●
PA4/PA5/PA6/PA7		-	-	-
PB12/PB13/PB14/PB15		-	-	●
PA15/PB3/PB4/PB5		-	-	-

The symbol “●” means the pin alternate functions are supported in the MCU(s).

The symbol “-” means the pin alternate functions are not supported in the MCU(s).

6.5 Others pin mapping

Table 6-9 Others pin mapping

GPIO Port	PMU	RCC	ADC Input	RTC
PA0	WKUP1	CKI_4	AIN0	RTC_TAMP2
PA1			AIN1	
PA2			AIN2	
PA3			AIN3	
PA4		CKI_1	AIN4	
PA5			AIN5	
PA6			AIN6	
PA7			AIN7	
PA8				
PA9				
PA10				
PA11				
PA12				
PA13		CKI_2		
PA14		CKI_3		
PA15				
PB0			AIN8	
PB1			AIN9	
PB2				
PB3				
PB4				
PB5				
PB6				
PB7				
PB8				
PB9				
PB10				
PB11				
PB12				
PB13				

GPIO Port	PMU	RCC	ADC Input	RTC
PB14				
PB15		RTC_REFIN		
PC0			AIN10	
PC1			AIN11	
PC2			AIN12	
PC3			AIN13	
PC4			AIN14	
PC6				
PC7				
PC8				
PC9				
PC10				
PC11				
PC12				
PC13	WKUP2	RTC_TAMP2 RTC_TS RTC_OUT		
PC14				
PC15		LSE_CK1		
PD2				
PF0		HSE_CK1		
PF1				
PF2				
PF3				
PF4				
PF5				
PF6				
PF7				

7 Package characteristics

7.1 LQFP64

LQFP64 is a 10 x 10 mm and 0.5 mm pitch package.

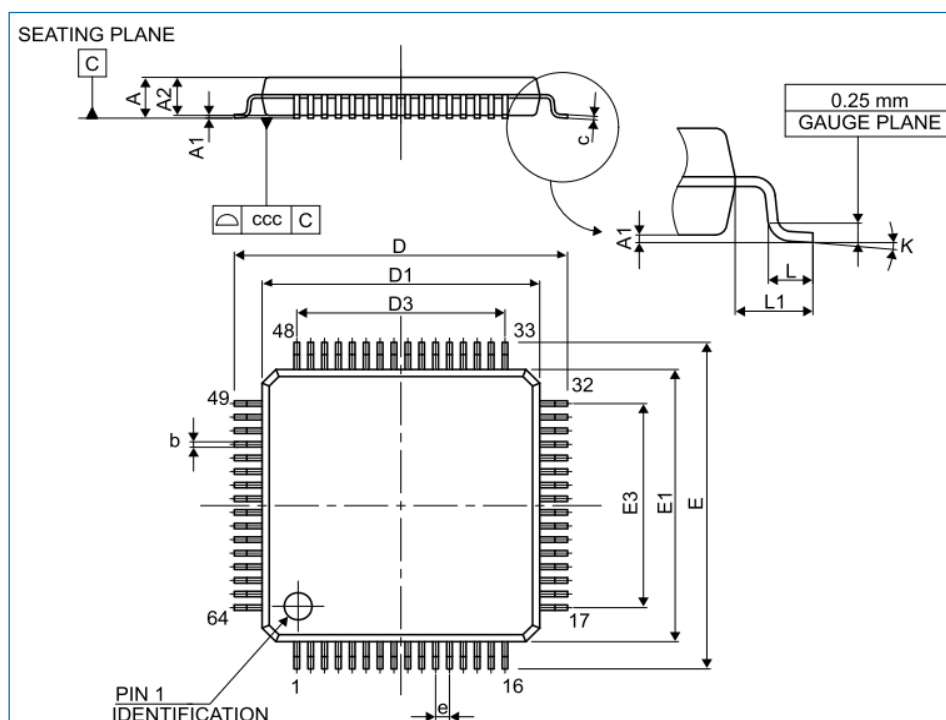


Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	Millimeters			Inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
B	0.170	0.220	0.270	0.0067	0.0087	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
E	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
Ccc	-	-	0.080	-	-	0.0031

(1) Values in inches are converted from mm and rounded to 4 decimal digits

7.2 LQFP48

LQFP48 is a 7 mm x 7 mm and 0.5 mm pitch package.

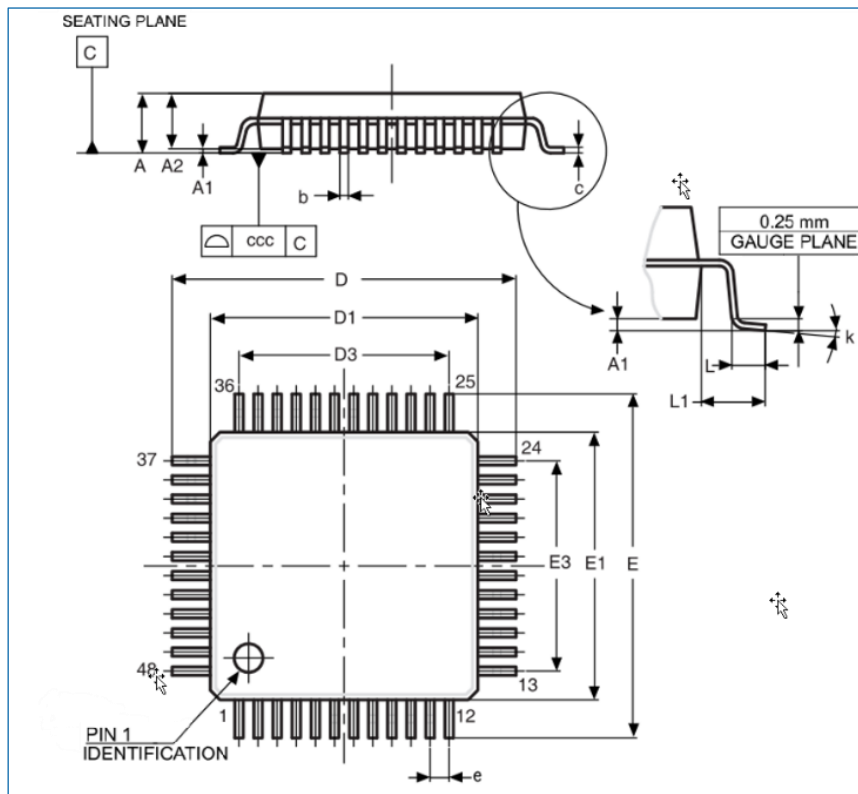


Figure 7-2 LQFP48 package outline

Table 7-2 LQFP48 package parameters

Symbol	millimeters			Inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
B	0.170	0.220	0.270	0.0067	0.0087	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
E	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
Ccc			0.080			0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 LQFP32

LQFP32 is a 7 mm x 7 mm and 0.8 mm pitch package.

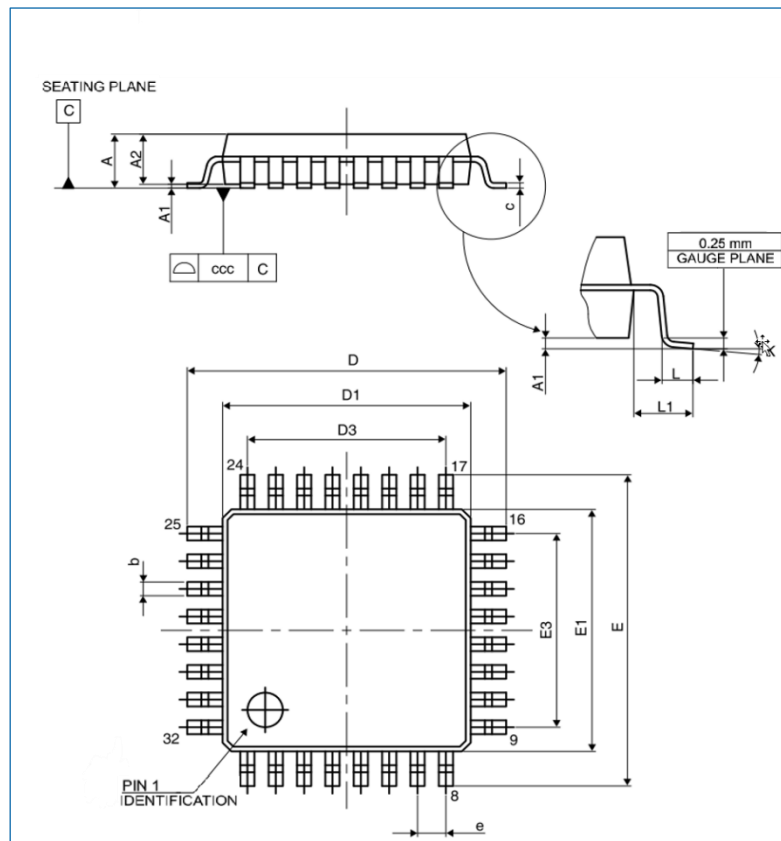


Figure 7-3 LQFP32 package outline

Table 7-3 LQFP32 package parameters

Symbol	millimeters			Inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
B	0.300	0.370	0.450	0.0118	0.0146	0.0177
C	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
E	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
Ccc	0.100			0.0039		

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

7.4 TSSOP20

TSSOP20 is a 6.5 mm x 4.4 mm and 0.65 mm pitch package.

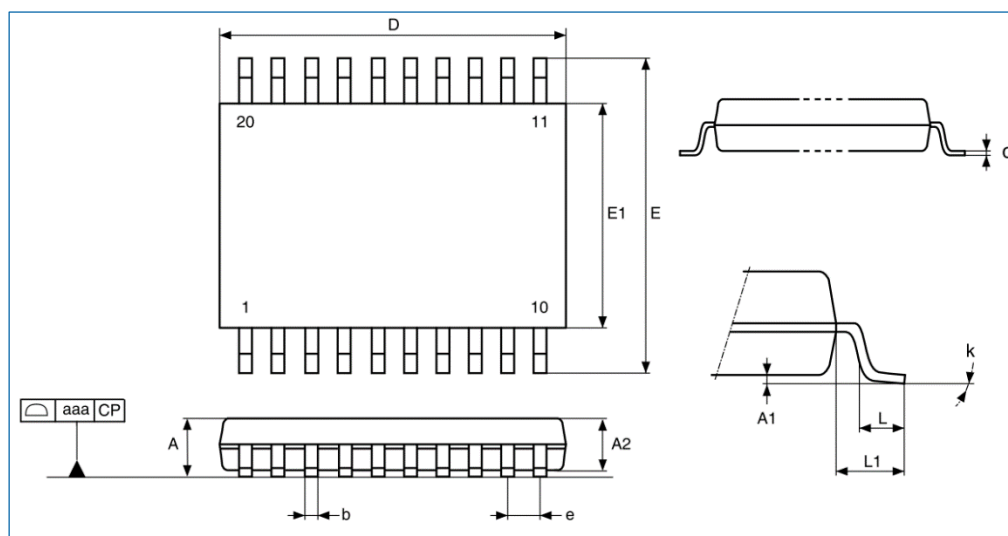


Figure 7-4 TSSOP20 package outline

Table 7-4 TSSOP20 package parameters

Symbol	millimeters			Inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
B	0.190	-	0.300	0.0075	-	0.0118
C	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
E	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	-	8.0°	0°	-	8.0°
Aaa	-	-	0.1000	-	-	0.0039

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

8 Ordering information

Table 8-1 HK32F030 ordering information

Package	MCU Name	Packaging	Comments
LQFP64	HK32F030R8T6	Tape and reel /Tray	-
LQFP48	HK32F030C8T6	Tape and reel/Tray	-
	HK32F030C6T6	Tape and reel/Tray	-
LQFP32	HK32F030K6T6	Tape and reel/Tray	-
TSSOP20	HK32F030F4P6	Tape and reel/Tray	-

9 Glossary and Abbreviations

Name	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EXTI	Extended Interrupts and Events Controller
FSMC	Flexible Static Memory Controller
GPIO	General Purpose Input Output
HSE	High Speed External (Clock Signal)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal (Clock Signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
WWDG	Window Watchdog

10 Legal and Contact Information



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